

## MEMORY HUB TESTER INTERFACE AND METHOD FOR USE THEREOF

### TECHNICAL FIELD

The present invention relates to systems and methods for testing memory devices, and more particularly, to systems and methods for testing memory devices through  
5 a system bridge to enable the use of a relatively low-speed tester to test higher speed memory devices.

### BACKGROUND OF THE INVENTION

Computer systems use memory devices, such as dynamic random access memory ("DRAM") devices, to store data that are accessed by a processor. These memory  
10 devices are normally used as system memory in a computer system. In a typical computer system, the processor communicates with the system memory through a processor bus and a memory controller. The memory devices of the system memory, typically arranged in memory modules having multiple memory devices, are coupled through a memory bus to the memory controller. The processor issues a memory request, which includes a memory  
15 command, such as a read command, and an address designating the location from which data or instructions are to be read. The memory controller uses the command and address to generate appropriate command signals as well as row and column addresses, which are applied to the system memory through the memory bus. In response to the commands and addresses, data are transferred between the system memory and the processor. The  
20 memory controller is often part of a system controller, which also includes bus bridge circuitry for coupling the processor bus to an expansion bus, such as a PCI bus.

In memory systems, high data bandwidth is desirable. Generally, bandwidth limitations are not related to the memory controllers since the memory controllers sequence data to and from the system memory as fast as the memory devices allow. One approach  
25 that has been taken to increase bandwidth is to increase the speed of the memory data bus coupling the memory controller to the memory devices. Thus, the same amount of

information can be moved over the memory data bus in less time. However, despite increasing memory data bus speeds, a corresponding increase in bandwidth does not result. One reason for the non-linear relationship between data bus speed and bandwidth is the hardware limitations within the memory devices themselves. That is, the memory controller has to schedule all memory commands to the memory devices such that the hardware limitations are honored. Although these hardware limitations can be reduced to some degree through the design of the memory device, a compromise must be made because reducing the hardware limitations typically adds cost, power, and/or size to the memory devices, all of which are undesirable alternatives. Thus, given these constraints, although it is easy for memory devices to move "well-behaved" traffic at ever increasing rates, for example, sequel traffic to the same page of a memory device, it is much more difficult for the memory devices to resolve "badly-behaved traffic," such as bouncing between different pages or banks of the memory device. As a result, the increase in memory data bus bandwidth does not yield a corresponding increase in information bandwidth.

In addition to the limited bandwidth between processors and memory devices, the performance of computer systems is also limited by latency problems that increase the time required to read data from system memory devices. More specifically, when a memory device read command is coupled to a system memory device, such as a synchronous DRAM ("SDRAM") device, the read data are output from the SDRAM device only after a delay of several clock periods. Therefore, although SDRAM devices can synchronously output burst data at a high data rate, the delay in initially providing the data can significantly slow the operating speed of a computer system using such SDRAM devices. Increasing the memory data bus speed can be used to help alleviate the latency issue. However, as with bandwidth, the increase in memory data bus speeds do not yield a linear reduction of latency, for essentially the same reasons previously discussed.

Although increasing memory data bus speed has, to some degree, been successful in increasing bandwidth and reducing latency, other issues are raised by this

approach. For example, as the speed of the memory data bus increases, loading on the memory bus needs to be decreased in order to maintain signal integrity since traditionally, there has only been wire between the memory controller and the memory slots into which the memory modules are plugged. Several approaches have been taken to accommodate the increase in memory data bus speed. For example, reducing the number of memory slots, adding buffer circuits on a memory module in order to provide sufficient fanout of control signals to the memory devices on the memory module, and providing multiple memory device interfaces on the memory module since there are too few memory module connectors on a single memory device interface. The effectiveness of these conventional approaches are, however, limited. A reason why these techniques were used in the past is that it was cost-effective to do so. However, when only one memory module can be plugged in per interface, it becomes too costly to add a separate memory interface for each required memory slot. In other words, it pushes the system controllers package out of the commodity range and into the boutique range, thereby, greatly adding cost.

One recent approach that allows for increased memory data bus speed in a cost effective manner is the use of multiple memory devices coupled to the processor through a memory hub. A computer system 100 shown in Figure 1 uses a memory hub architecture. The computer system 100 includes a processor 104 for performing various computing functions, such as executing specific software to perform specific calculations or tasks. The processor 104 includes a processor bus 106 that normally includes an address bus, a control bus, and a data bus. The processor bus 106 is typically coupled to cache memory 108, which, is typically static random access memory ("SRAM"). Finally, the processor bus 106 is coupled to a system controller 110, which is also sometimes referred to as a bus bridge. The system controller 110 serves as a communications path to the processor 104 for a variety of other components. For example, as shown in Figure 1, the system controller 110 includes a graphics port that is typically coupled to a graphics controller 112, which is, in turn, coupled to a video terminal 114. The system controller 110 is also coupled to one or more input devices 118, such as a keyboard or a mouse, to

allow an operator to interface with the computer system 100. Typically, the computer system 100 also includes one or more output devices 120, such as a printer, coupled to the processor 104 through the system controller 110. One or more data storage devices 124 are also typically coupled to the processor 104 through the system controller 110 to allow the processor 104 to store data or retrieve data from internal or external storage media (not shown). Examples of typical storage devices 124 include hard and floppy disks, tape cassettes, and compact disk read-only memories (CD-ROMs).

The system controller 110 includes a memory hub controller 128 that is coupled to the processor 104. The system controller 110 is further coupled over a high speed bi-directional or unidirectional system controller/hub interface 134 to several memory modules 130a-n. Typically, the memory modules 130a-n are coupled in a point-to-point or daisy chain architecture such that the memory modules 130a-n are connected one to another in series. Thus, the system controller 110 is coupled to a first memory module 130a, with the first memory module 130a connected to a second memory module 130b, and the second memory module 130b coupled to a third memory module 130c, and so on in a daisy chain fashion. Each memory module 130a-n includes a memory hub 140 that is coupled to the system controller/hub interface 134, and is further coupled a number of memory devices 148 through command, address and data buses, collectively shown as bus 150. The memory hub 140 efficiently routes memory requests and responses between the memory hub controller 128 and the memory devices 148.

The memory devices 148 on the memory modules 130a-n are typically capable of operating at high clock frequencies in order to facilitate the relatively high speed operation of the overall memory system. Consequently, computer systems employing this architecture can also use the high-speed system controller/hub interface 134 to complement the high clock speeds of the memory devices 148. Additionally, with a memory hub based system, signal integrity can be maintained on the system controller/hub interface 134 since the signals are typically transmitted through multiple memory hubs 140 to and from the memory hub controller 128. Moreover, this architecture also provides for easy expansion

of the system memory without concern for degradation in signal quality as more memory modules are added, such as occurs in conventional memory bus architectures.

It will be appreciated that testing the memory devices 148 of the memory modules 130a-n typically requires the use of test equipment that can accommodate the high clock frequencies under which the memory devices 148 operate. That is, the testers, test interface equipment, and the like are designed to perform various tests on the memory devices 148 to determine the functionality of the devices under typical operating conditions. For example, testers should be able to generate test signals, such as command, address, and data signals, with sufficient signal accuracy and at least at the speed under which the memory devices 148 operate in order to perform meaningful testing. Additionally, the tester should preferably be able to analyze the relative timing margin for various aspects of the memory devices 148 in operation, which typically requires the tester to operate at clock frequencies higher than which the memory devices 148 operate. Although such test equipment is available, the economic costs to purchase this equipment is often very high. The burden is greatly increased in a manufacturing setting, where multiple test equipment is required to maintain adequate production throughput. Consequently, if the costs of the test equipment are prohibitive, the quality of memory device testing will be compromised or production output will suffer, neither of which is a desirable solution. Therefore, there is a need for systems and methods that provide alternative approaches to testing memory devices.

## SUMMARY OF THE INVENTION

A memory hub according to one aspect of the invention includes a memory test bridge circuit having a tester interface through which test command packets are received responsive to a test clock signal and further having a memory interface coupled to the tester interface through which memory commands corresponding to a test command packet are provided to at least one memory device responsive to a memory clock signal. The memory hub further includes an error detect circuit coupled to the memory test bridge

circuit for comparing expected data received by the memory test bridge circuit to read data returned from the memory device in response to a memory command, the error detect circuit operable to generate in response to the comparison pass/fail data indicative of whether the read data matches the expected data.

5                In another aspect of the invention, a method for testing a memory device is provided including coupling test command packets from a tester to a memory hub responsive to a test clock signal having a test clock frequency, generating in the memory hub memory device command, address, and data signals in accordance with the test command packets, and coupling the memory device command, address, and data signals  
10    from the memory hub to a memory device under test responsive to a memory device clock signal having a memory device clock frequency.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a partial block diagram of a processor-based system having system memory that uses a conventional memory hub architecture.

15                Figure 2 is a partial block diagram of a test apparatus for testing memory device having a memory hub according to an embodiment of the present invention.

Figure 3 is a partial block diagram of a memory hub according to an embodiment of the present invention.

20                Figure 4 is partial timing diagram for a test apparatus including a memory hub according to an embodiment of the present invention.

Figure 5 is a diagram of a test command packet data structure for a memory hub according to an embodiment of the present invention.

Figure 6 is a diagram of a test command packet data structure for a memory hub according to another embodiment of the present invention.

25                Figure 7 is a partial block diagram of a test apparatus for testing a memory module for use in a hub-based memory system having a memory hub according to an embodiment of the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

Figure 2 illustrates a memory device test arrangement 200 according to an embodiment of the present invention. A conventional tester 202, as known in the art, is coupled to a memory hub 210 through a tester/memory hub bus 204. The tester/memory hub bus 204 includes an uplink bus 208 coupled to the hub 210 through which test command packets are provided to the memory hub 210, and further includes a test control bus 206 through which the testing can be controlled and monitored as well as through which test results can be obtained. The memory hub is coupled to a plurality of memory devices 212a-h through respective memory busses 220a-h. As will be described in more detail below, the test command packets provided by the tester 202 to the memory hub 210 include information for performing testing of the memory devices 212a-h, such as memory commands, test addresses, test data, and the like. Although the memory hub 210 is shown in Figure 2 as being coupled to each of the memory devices 212a-h through a respective memory bus 220a-h, it will be appreciated that the memory hub 210 and memory devices 212a-h can be coupled through a common memory bus (not shown) as well. The memory busses 220a-h include signal lines for coupling memory addresses, memory commands, and data between the memory hub 210 and the memory devices 212a-h.

As will be explained in greater detail below, the memory hub 210 acts as a "test bridge" between the tester 202 and the memory devices 212a-h. In this manner, a tester having a maximum operating clock frequency that is less than that of the operating clock frequency of the memory devices 212a-h can still be used to test the memory devices 212a-h at their operating clock frequency. Generally, the tester 202 drives test patterns to various degrees, and the memory hub 210 drives the high speed interface electronics coupled to the memory devices 212a-h.

Figure 3 illustrates a portion of a memory hub 300. The memory hub 300 can be substituted for the memory hub 210 shown in Figure 2. A multiplexer 302 is coupled to the uplink bus 208, which is shown in Figure 3 as having a first uplink LINKIN0 208a and a second uplink LINKIN1 208b. The multiplexer 302 selects between

the uplink 208a and 208b to be coupled to a memory hub test command bus 304. Coupled to the memory hub test command bus 304 are test command latch 310, test address latch 312 and test address opcode latch 314, and test data latch 316 and test data opcode latch 318. The latches 310, 312, 314, 316, 318 are conventional, and as will be explained in more detail below, latch various signals of the test command packet provided to the memory hub 210 from the tester 202 (Figure 2).

A test address arithmetic and logic unit (ALU) 324 coupled to the test address latch 312 performs arithmetic and logical operations on test addresses according to a test address opcode latched by the test address opcode latch 314. As will be explained in more detail below, the test address opcode is provided to the memory hub 300 as part of the test command packet. The output of the test address ALU 324 is coupled back through a multiplexer 330 to the test address latch 312 in the event the test address ALU 324 is instructed to perform operations on a test address resulting from a previous test address ALU operation. The test address latch 312, test address opcode latch 314, the test address ALU 324, and the multiplexer 330 generally define a test address generator 340. The memory hub 210 further includes a test data ALU 326 coupled to the test data latch 316 for performing arithmetic and logical operations on test data according to a test data opcode latched by the test data opcode latch 318. As will be explained in more detail below, the test data opcode is provided to the memory hub 300 as part of the test command packet. The output of the test data ALU 326 is coupled back through a multiplexer 332 to the test data latch 316 in the event the test data ALU 326 is instructed to perform operations on test data resulting from a previous test data ALU operation. The test data latch 316, test data opcode latch 318, test data ALU 326, and the multiplexer 332 generally define a test data generator 350.

A memory address interface latch 360 is coupled to the test address ALU 324 to provide a test address to the memory devices 212a-h (Figure 2). Similarly, a memory data interface latch 364 coupled to the output of the test data ALU 326 provides test data to the memory devices 212a-h. A memory command interface latch 362 coupled

to the test command latch 310 to provide memory commands to the memory devices 212a-h. Each of the memory interface latches 360, 362, 364 are coupled to the corresponding signal lines of the memory busses 220a-h.

Also included in the memory hub 210 are error detect logic 370 and a data  
5 capture buffer 372 coupled to the data signal lines of the memory busses 220a-h. As shown in Figure 3, the error detect logic 370 and the data capture buffer 372 are coupled to data bus distinct from the data bus to which the memory data interface latch 364 is coupled. However, it will be appreciated that Figure 3 is representative, and that the data busses to which the error detect logic 370, the data capture buffer 372, and the memory data interface  
10 latch 364 are coupled can be a bi-directional bus, as known in the art. More generally, the memory interface latches 360, 362, 364 represent a memory interface circuit to which, the error detect logic 370 and the data capture buffer 372 are coupled.

The error detect logic 370 includes logic to compare the data read from the memory devices 212a-h with the expected data written to the memory devices 212a-h  
15 in order to determine whether a memory device 212a-h passes or fails testing. The error detect logic 370 includes test result registers (not shown) that store information indicative of the results of the comparison which are accessible to the tester 202. In this manner, the results of testing the memory devices 212a-h can be provided to the tester 202 when requested. A capture buffer 372 is also coupled to the data signal lines of the memory  
20 busses 220a-h to store read data from the memory devices 212a-h in the event that review of particular read data by the tester 202 is desired. For example, where an error has been detected by the error detect logic 370, it may be desirable for the tester 202 to review the particular data that caused the error by retrieving it from the capture buffer 372. A multiplexer 374 is coupled to the error detect logic 370 and the capture buffer 372 to select  
25 between providing the information indicative of test results or particular read data to the tester 202. It will be appreciated that in alternative embodiments, the information from the capture buffer 372 and the error detect logic 370 can be provided to the tester 202 directly, rather than through the multiplexer 374. Alternative arrangements for providing test results

or particular read data to the tester 202 can also be utilized without departing from the scope of the present invention.

It will be appreciated that the previously described circuitry can be included in the memory hub 210 specifically for testing purposes, or alternatively, various circuits included in the memory hub 210 for normal operation can be utilized where appropriate. For example, the test command latch 310 can be replaced by a command latch used during normal operation of the memory hub 210. Similarly, the test address generator 340, although described with respect to Figure 3 as being included for testing purposes, can be replaced by address circuitry already included in the memory hub 210 for use during normal operation. Such modifications can be made without departing from the scope of the present invention.

In operation, memory test command packets are provided to the memory hub 300 in parallel over the first and second uplink busses 208a, 208b every clock cycle of a test clock. The memory test command packets are then de-multiplexed and the test command, address, and data information included in the test command packets are latched by the corresponding test command, address, and data latches 310, 312, and 318, according to a faster memory clock frequency. The test command, address, and data information are then converted into the appropriate signals for the memory devices 212a-h and latched by the respective memory address, command, and data interface latches 360, 362, 364. Thus, the link interface behaves as a multiplexed memory device command bus. In this manner, a tester can provide test command packets in parallel to the memory hub 300 at a first clock frequency over the first and second uplink busses 208a, 208b, and the memory devices 212a-h can receive memory test commands at a second clock frequency over the memory busses 220a-h in order to test at a different, typically higher, clock frequency. As a result, enough test command throughput for the higher speed memory devices 212a-h are provided through the memory hub 300, which allows for considerable flexibility for command scheduling.

Figure 4 is a timing diagram illustrating the latching of test command packets and provision to the memory interface latches 360, 362, and 364. At a time T0, the test command, address and data information included with a test command packet is latched. At a time T1, the information, now converted into the appropriate signals for the memory devices, is latched by the test address, command, and data interface latches 360, 362, 364 and provided to the memory devices 212a-h under test. It will be appreciated that at the time T1, although not shown in Figure 4, the test command, address and data information for the next test command packet can be latched. Thus, the latching of test command, address, and data information, and provision of appropriate memory signals to the memory devices 212a-h can be interleaved so that for each clock cycle, a test command can be provided to the memory devices 212a-h.

As previously discussed, in response to receiving the memory test command packets, the appropriate test command, address, and data information is latched by the respective test latches, 310, 312, and 318. In the embodiment shown in Figure 3, test memory addresses and test data may be provided as part of the test command packet. Alternatively, address ALU opcodes and test data ALU opcodes can be provided for operation of the test address ALU 324 and the test data ALU 326. That is, rather than provide the test address and test data information directly in the test command packet, the test address and test data for testing the memory devices can be generated by test address generator 340 and the test data generator 350 included in the memory hub 300.

Figure 5 illustrates a test command packet data structure 500 that can be used with a memory hub having the test address and test data generators 340, 350. The test command packet 500 is 16-bits in length, with the three least significant bits <2:0> representing the test command field 504 for test command information, three bits <5:3> representing the test address ALU opcode field 508, two bits <7:6> representing the test data ALU opcode field 512, and eight bits <15:8> representing repeat operation field 516 for repeat operation instructions.

Various types of opcodes known in the art can be used with the test address ALU 324 and the test data ALU 326 for testing the memory devices 212a-h. For example, the types of opcodes that may be desirable for the test address ALU 324 include an INCREMENT command for incrementing a current address latched by the address latch 312, a DECREMENT command for decrementing a current address in the address latch 312, a COMPLEMENT command to complement the bits of a current address, a RESET command to set all the bits of a current address to zero, a SET command to set all the bits of a current address to one, and a NOOP command to not perform any operation on a current address. With respect to the opcodes for the test data ALU 326, it may be desirable to have a RESET command to set a current data value latched in the test data latch 318 to zero, a SET command to set a current data value to one, a COMPLEMENT command to complement a current data value, and a NOOP command to not perform any operation on a current data value. The types of instructions that may be desirable for the repeat operation field 516 can include instructions such as NO\_REPEAT to carry out the test address and data operations only once, REPEAT\_n to repeat the test address and data operations n times, n being a value provided with the repeat operation instruction, REPEAT\_CONTINUE to repeat the test address and data operations indefinitely, and REPEAT\_STOP to discontinue repeating the test address and data operations. Programming such opcodes and repeat operation instructions are well known in the art, and can be implemented using conventional hardware and software designs.

It will be appreciated that the particular embodiment of the memory test command packet illustrated in Figure 5 has been provided by way of an example, and that the particular fields 504, 508, 512, 516 included in a memory test command packet 500, as well as the bit-length of the fields 504, 508, 512, 516, can be modified without departing from the scope of the present invention. Moreover, the types of opcodes that can be used for the test address ALU 324 and the test data ALU 326 and the repeat operation instructions are generally known to those ordinarily skilled in the art, and consequently, the opcodes and repeat operation instructions described herein for particular embodiments of

the present invention can be modified without departing from the scope of the present invention.

Figure 6 illustrates a test command packet 600 for an alternative embodiment of a memory hub 210 (Figure 2) having memory device test capabilities. As shown in Figure 6, the test command packet 600 is 16-bits, with the three least significant bits  $\langle 2:0 \rangle$  representing the memory commands for the memory devices 212a-h, and the remaining 13-bits  $\langle 15:3 \rangle$  representing a 13-bit memory address for the memory devices 212a-h. Test data is provided to the memory hub 210, and further onto the memory devices 212a-h in a conventional manner. That is, the test data, when appropriate, is provided to the memory hub 210 over the uplink bus 208. The memory hub 210, which receives the test data, along with the test command packet 600, forwards the test data onto the memory devices 212a-h using the respective memory busses 220a-h. In contrast to the embodiment of the memory hub 300 shown in Figure 3, rather than provide a test command packet having a test command, and instructions for generating test addresses and test data in the memory hub 300, the test command packet 600 provides the test command and the test address directly to the memory hub, which is then translated into the appropriate signals for testing the memory devices 212a-h. As further shown in Figure 6, the test command packet 600 is latched by the memory hub 210 at a time  $T_0$ , with a next test command packet 604 latched the next clock cycle at a time  $T_1$ . Test command packets 608 and 612 are latched at the next two clock cycles at times  $T_2$  and  $T_3$ . Thus, as shown in Figure 6, a test command packet can be provided to the memory device 212a-h at each clock cycle. As previously discussed with respect to the memory hub 300, test command packets having the format shown in Figure 6 are provided to the memory hub in parallel over the first and second uplink busses 208a, 208b every clock cycle of a tester clock signal. The memory test commands are then de-multiplexed and provided to the memory devices 212a-h by the memory hub according to a memory clock signal having a second, typically higher, clock frequency. In this manner, the memory devices 212a-h can be tested at a higher frequency

memory clock signal, although the tester 202 is providing the test command packets to the memory hub 210 according to a lower frequency test clock signal.

In an alternative embodiment, at least one of the test address and test data generators is included in the memory hub 210 (Figure 2), with the test command packet including test ALU commands for the test generator that is present in the memory hub 210, and the test command packet further including the other test information to be provided directly to the memory hub 210.

Figure 7 illustrates a test apparatus 700 for testing memory devices 148 of a memory module 130 for use in a hub-based memory system. The test apparatus 700 includes a memory tester 702 having a tester/memory hub interface circuit 704. The memory tester 702 is coupled to a memory hub 740 located on the memory module 130 through a test control bus 708 and an test uplink bus 710. The memory hub 740 is coupled to the memory devices 148 through memory device command, address and data buses, collectively shown as busses 150. The memory hub 740 includes memory test circuits 742 according to embodiments of the present invention for testing the memory devices 148. The memory devices 148 are tested according to a memory device clock signal although the memory hub 740 receives test command packets over the test uplink bus 710 according to a tester clock signal. The tester clock signal has a first clock frequency and the memory device clock signal has a second clock frequency that is generally higher than the first clock frequency.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

## CLAIMS

## 1. A memory hub, comprising:

a test command interface for coupling to a test bus and through which test command packets are received, the test command interface configured to latch the test command packets in response to a test clock signal having a test clock frequency;

a memory device interface for coupling memory device command, address and data signals to a memory device, the memory device interface configured to provide the memory device command, address and data signals to the memory device in response to a memory device clock signal having a memory device clock frequency;

a test command latch coupled to the test command interface and the memory device interface to latch a memory device command of a received test command packet and provide memory device command signals to the memory device in accordance with the memory device command to test the memory device;

a test address generator coupled to the test command interface and the memory device interface to generate the memory device address signals for the memory device in accordance with the received test command packet;

a test data generator coupled to the test command interface and the memory device interface to generate the memory device data signal for the memory device in accordance with the received test command packet; and

an error detect circuit coupled to the test bus and configured to compare expected data corresponding to the memory device data signal and data read from the memory device and further configured to provide a signal indicative of the results from the comparison over the test bus.

2. The memory hub of claim 1 wherein the test command packet comprises test command, test address, and test data signals, the test address signals representative of a memory device address and the test data signals representative of memory device data.

3. The memory hub of claim 1 wherein the test command packet comprises test command and test address ALU opcode signals, the test address ALU opcode signals representative of at least one of arithmetic and logic operations performed to generate memory device address signals.

4. The memory hub of claim 1 wherein the test command packet comprises test command and test data ALU opcode signals, the test data ALU opcode signals representative of at least one of arithmetic and logic operations performed to generate memory device data signals.

5. The memory hub of claim 1, further comprising a capture buffer coupled to the test bus and the memory device, the capture buffer configured to capture data read from the memory device and provide the same over the test bus when requested.

6. The memory hub of claim 1 wherein the test command interface is coupled to the test bus having a plurality of uplinks on which a plurality of test command packets are received by the test command interface concurrently.

7. The memory hub of claim 6 wherein the test command interface includes a multiplexer coupled to the plurality of uplinks to multiplex between the plurality of uplinks in providing the memory device command, address, and data signals to the memory device.

8. The memory hub of claim 1 wherein the test address generator comprises:  
a test address latch to latch test address information;  
a test address arithmetic and logic unit (ALU) opcode latch to latch a test address ALU opcode included with the test command packet; and

a test address ALU coupled to the test address latch and the test address ALU opcode latch for performing at least one of arithmetic and logic operations on the test address information in accordance with the test address opcode.

9. The memory hub of claim 1 wherein the test data generator comprises:

a test data latch to latch test data information;

a test data arithmetic and logic unit (ALU) opcode latch to latch a test data ALU opcode included with the test command packet; and

a test data ALU coupled to the test data latch and the test data ALU opcode latch for performing at least one of arithmetic and logic operations on the test data information in accordance with the test data opcode.

10. The memory hub of claim 1 wherein the memory device interface comprises a memory device command latch, a memory device address latch and a memory device data latch for latching the memory device command, address, and data signals.

11. The memory hub of claim 1 wherein the test clock frequency is less than the memory device clock frequency.

12. A memory hub, comprising:

a test circuit having a test command packet latch to latch test command packets including test command information, the test circuit latching the test command packets responsive to a test clock signal having a test clock frequency, the test interface circuit further having a test command circuit coupled to the test command packet latch to generate memory device command, address and data signals for testing a memory device in accordance with the test command information;

a memory device interface circuit coupled to the test circuit to couple the memory device command, address and data signals to a memory device under test, the memory device

interface configured to provide the memory device command, address and data signals to the memory device under test responsive to a memory device clock signal having a memory device clock frequency; and

an error detect circuit coupled to the memory device interface circuit and the test circuit to compare expected data corresponding to the memory device data signal and data read from the memory device under test, the error detect circuit configured to provide a signal indicative of the results from the comparison for access through the test circuit.

13. The memory hub of claim 12 wherein the test command packet comprises test command, test address, and test data signals, the test address signals representative of a memory device address and the test data signals representative of memory device data.

14. The memory hub of claim 12 wherein the test command packet comprises test command and test address ALU opcode signals, the test address ALU opcode signals representative of at least one of arithmetic and logic operations performed to generate memory device address signals.

15. The memory hub of claim 12 wherein the test command packet comprises test command and test data ALU opcode signals, the test data ALU opcode signals representative of at least one of arithmetic and logic operations performed to generate memory device data signals.

16. The memory hub of claim 12, further comprising a capture buffer coupled to the test circuit and the memory device interface, the capture buffer configured to capture data read from the memory device under test and provide the same through the test circuit when requested.

17. The memory hub of claim 12 wherein the test circuit is coupled to a plurality of uplinks on which a plurality of test command packets are received by the test circuit concurrently.

18. The memory hub of claim 17 wherein the test circuit includes a multiplexer coupled to the plurality of uplinks to multiplex between the plurality of uplinks in providing the memory device command, address, and data signals to the memory device.

19. The memory hub of claim 12 wherein the test circuit includes a test address generator comprising:

- a test address latch to latch test address information;

- a test address arithmetic and logic unit (ALU) opcode latch to latch a test address ALU opcode included with the test command packet; and

- a test address ALU coupled to the test address latch and the test address ALU opcode latch for performing at least one of arithmetic and logic operations on the test address information in accordance with the test address opcode.

20. The memory hub of claim 12 wherein the test circuit includes a test data generator comprising:

- a test data latch to latch test data information;

- a test data arithmetic and logic unit (ALU) opcode latch to latch a test data ALU opcode included with the test command packet; and

- a test data ALU coupled to the test data latch and the test data ALU opcode latch for performing at least one of arithmetic and logic operations on the test data information in accordance with the test data opcode.

21. The memory hub of claim 12 wherein the memory device interface comprises a memory device command latch, a memory device address latch and a memory device data latch for latching the memory device command, address, and data signals.

22. The memory hub of claim 12 wherein the test clock frequency is less than the memory device clock frequency.

23. A memory hub, comprising:

a memory test bridge circuit having a tester interface through which test command packets are received responsive to a test clock signal and further having a memory interface coupled to the tester interface through which memory commands corresponding to a test command packet are provided to at least one memory device responsive to a memory clock signal; and

an error detect circuit coupled to the memory test bridge circuit for comparing expected data received by the memory test bridge circuit to read data returned from the memory device in response to a memory command, the error detect circuit operable to generate in response to the comparison pass/fail data indicative of whether the read data matches the expected data.

24. The memory hub of claim 23 wherein the test command packet comprises test command, test address, and test data signals, the test address signals representative of a memory device address and the test data signals representative of memory device data.

25. The memory hub of claim 23 wherein the test command packet comprises test command and test address ALU opcode signals, the test address ALU opcode signals representative of at least one of arithmetic and logic operations performed to generate memory device address signals.

26. The memory hub of claim 23 wherein the test command packet comprises test command and test data ALU opcode signals, the test data ALU opcode signals representative of at least one of arithmetic and logic operations performed to generate memory device data signals.

27. The memory hub of claim 23, further comprising a capture buffer coupled to the memory test bridge circuit, the capture buffer configured to capture data read from the memory device and provide the same when requested.

28. The memory hub of claim 23 wherein the memory test bridge circuit is coupled to a plurality of uplinks on which a plurality of test command packets are received by the memory test bridge concurrently.

29. The memory hub of claim 28 wherein the memory test bridge circuit includes a multiplexer coupled to the plurality of uplinks to multiplex between the plurality of uplinks in providing the memory device command, address, and data signals to the memory device.

30. The memory hub of claim 23 wherein the memory test bridge circuit includes a test address generator comprising:

- a test address latch to latch test address information;

- a test address arithmetic and logic unit (ALU) opcode latch to latch a test address ALU opcode included with the test command packet; and

- a test address ALU coupled to the test address latch and the test address ALU opcode latch for performing at least one of arithmetic and logic operations on the test address information in accordance with the test address opcode.

31. The memory hub of claim 23 wherein the memory test bridge circuit includes a test data generator comprising:

a test data latch to latch test data information;

a test data arithmetic and logic unit (ALU) opcode latch to latch a test data ALU opcode included with the test command packet; and

a test data ALU coupled to the test data latch and the test data ALU opcode latch for performing at least one of arithmetic and logic operations on the test data information in accordance with the test data opcode.

32. The memory hub of claim 23 wherein the memory interface of the memory test bridge circuit comprises a memory device command latch, a memory device address latch and a memory device data latch for latching the memory device command, address, and data signals.

33. The memory hub of claim 23 wherein the test clock signal has a test clock frequency that is less than a memory device clock signal of the memory device clock frequency.

34. A memory module, comprising:

a plurality of memory devices;

a memory device bus coupled to the memory devices; and

a memory hub coupled to the memory device bus, the memory hub comprising:

a test circuit having a test command packet latch to latch test command packets including test command information, the test circuit latching the test command packets responsive to a test clock signal having a test clock frequency, the test interface circuit further having a test command circuit coupled to the test command packet latch to generate memory device command, address and data signals for testing a memory device in accordance with the test command information;

a memory device interface circuit coupled to the test circuit to couple the memory device command, address and data signals to a memory device under test, the memory device interface configured to provide the memory device command, address and data signals to the memory device under test responsive to a memory device clock signal having a memory device clock frequency; and

an error detect circuit coupled to the memory device interface circuit and the test circuit to compare expected data corresponding to the memory device data signal and data read from the memory device under test, the error detect circuit configured to provide a signal indicative of the results from the comparison for access through the test circuit.

35. The memory module of claim 34 wherein the test command packet comprises test command, test address, and test data signals, the test address signals representative of a memory device address and the test data signals representative of memory device data.

36. The memory module of claim 34 wherein the test command packet comprises test command signals, test address ALU opcode signals representative of at least one of arithmetic and logic operations performed to generate memory device address signals, and test data ALU opcode signals representative of at least one of arithmetic and logic operations performed to generate memory device data signals.

37. The memory module of claim 34 wherein the memory hub further comprises a capture buffer coupled to the test circuit and the memory device interface, the capture buffer configured to capture data read from the memory device under test and provide the same through the test circuit when requested.

38. The memory module of claim 34 wherein the test circuit of the memory hub is coupled to a plurality of uplinks on which a plurality of test command packets are received by the test circuit concurrently.

39. The memory module of claim 38 wherein the test circuit of the memory hub includes a multiplexer coupled to the plurality of uplinks to multiplex between the plurality of uplinks in providing the memory device command, address, and data signals to the memory device.

40. The memory module of claim 34 wherein the test circuit of the memory hub includes a test address generator comprising:

- a test address latch to latch test address information;

- a test address arithmetic and logic unit (ALU) opcode latch to latch a test address ALU opcode included with the test command packet; and

- a test address ALU coupled to the test address latch and the test address ALU opcode latch for performing at least one of arithmetic and logic operations on the test address information in accordance with the test address opcode.

41. The memory module of claim 34 wherein the test circuit of the memory hub includes a test data generator comprising:

- a test data latch to latch test data information;

- a test data arithmetic and logic unit (ALU) opcode latch to latch a test data ALU opcode included with the test command packet; and

- a test data ALU coupled to the test data latch and the test data ALU opcode latch for performing at least one of arithmetic and logic operations on the test data information in accordance with the test data opcode.

42. The memory module of claim 34 wherein the memory device interface of the memory hub comprises a memory device command latch, a memory device address latch and a memory device data latch for latching the memory device command, address, and data signals.

43. The memory module of claim 34 wherein the test clock frequency is less than the memory device clock frequency.

44. A memory module, comprising:

a plurality of memory devices;

a memory device bus coupled to the memory devices; and

a memory hub coupled to the memory device bus, the memory hub comprising:

a memory test bridge circuit having a tester interface through which test command packets are received responsive to a test clock signal and further having a memory interface coupled to the tester interface through which memory commands corresponding to a test command packet are provided to at least one memory device responsive to a memory clock signal; and

an error detect circuit coupled to the memory test bridge circuit for comparing expected data received by the memory test bridge circuit to read data returned from the memory device in response to a memory command, the error detect circuit operable to generate in response to the comparison pass/fail data indicative of whether the read data matches the expected data.

45. The memory module of claim 44 wherein the test command packet comprises test command, test address, and test data signals, the test address signals representative of a memory device address and the test data signals representative of memory device data.

46. The memory module of claim 44 wherein the test command packet comprises test command signals, test address ALU opcode signals representative of at least one of arithmetic and logic operations performed to generate memory device address signals, and test data ALU opcode signals representative of at least one of arithmetic and logic operations performed to generate memory device data signals.

47. The memory module of claim 44 wherein the memory hub further comprises a capture buffer coupled to the memory test bridge circuit, the capture buffer configured to capture data read from the memory device and provide the same when requested.

48. The memory module of claim 44 wherein the memory test bridge circuit of the memory hub is coupled to a plurality of uplinks on which a plurality of test command packets are received by the memory test bridge concurrently.

49. The memory module of claim 48 wherein the memory test bridge circuit of the memory hub includes a multiplexer coupled to the plurality of uplinks to multiplex between the plurality of uplinks in providing the memory device command, address, and data signals to the memory device.

50. The memory module of claim 44 wherein the memory test bridge circuit of the memory hub includes a test address generator comprising:

- a test address latch to latch test address information;

- a test address arithmetic and logic unit (ALU) opcode latch to latch a test address ALU opcode included with the test command packet; and

- a test address ALU coupled to the test address latch and the test address ALU opcode latch for performing at least one of arithmetic and logic operations on the test address information in accordance with the test address opcode.

51. The memory module of claim 44 wherein the memory test bridge circuit of the memory hub includes a test data generator comprising:

a test data latch to latch test data information;

a test data arithmetic and logic unit (ALU) opcode latch to latch a test data ALU opcode included with the test command packet; and

a test data ALU coupled to the test data latch and the test data ALU opcode latch for performing at least one of arithmetic and logic operations on the test data information in accordance with the test data opcode.

52. The memory module of claim 44 wherein the memory interface of the memory test bridge circuit comprises a memory device command latch, a memory device address latch and a memory device data latch for latching the memory device command, address, and data signals.

53. The memory module of claim 44 wherein the test clock signal has a test clock frequency that is less than a memory device clock signal of the memory device clock frequency.

54. A memory test apparatus, comprising:

a memory tester for providing memory test command packets to test memory devices;

a memory test bus coupled to the memory tester;

a memory module coupled to the memory test bus for testing, the memory module comprising:

a plurality of memory devices;

a memory device bus coupled to the memory devices; and

a memory hub coupled to the memory device bus, the memory hub comprising:

a test circuit having a test command packet latch to latch test command packets including test command information, the test circuit latching the test command packets responsive to a test clock signal having a test clock frequency, the test interface circuit further having a test command circuit coupled to the test command packet latch to generate memory device command, address and data signals for testing a memory device in accordance with the test command information;

a memory device interface circuit coupled to the test circuit to couple the memory device command, address and data signals to a memory device under test, the memory device interface configured to provide the memory device command, address and data signals to the memory device under test responsive to a memory device clock signal having a memory device clock frequency; and

an error detect circuit coupled to the memory device interface circuit and the test circuit to compare expected data corresponding to the memory device data signal and data read from the memory device under test, the error detect circuit configured to provide a signal indicative of the results from the comparison for access through the test circuit.

55. The memory test apparatus of claim 54 wherein the test command packet comprises test command, test address, and test data signals, the test address signals representative of a memory device address and the test data signals representative of memory device data.

56. The memory test apparatus of claim 54 wherein the test command packet comprises test command signals, test address ALU opcode signals representative of at least one of arithmetic and logic operations performed to generate memory device address signals, and test data ALU opcode signals representative of at least one of arithmetic and logic operations performed to generate memory device data signals.

57. The memory test apparatus of claim 54 wherein the memory hub further comprises a capture buffer coupled to the test circuit and the memory device interface, the capture buffer configured to capture data read from the memory device under test and provide the same through the test circuit when requested.

58. The memory test apparatus of claim 54 wherein the test circuit of the memory hub is coupled to a plurality of uplinks on which a plurality of test command packets are received by the test circuit concurrently.

59. The memory test apparatus of claim 58 wherein the test circuit of the memory hub includes a multiplexer coupled to the plurality of uplinks to multiplex between the plurality of uplinks in providing the memory device command, address, and data signals to the memory device.

60. The memory test apparatus of claim 54 wherein the test circuit of the memory hub includes a test address generator comprising:

- a test address latch to latch test address information;

- a test address arithmetic and logic unit (ALU) opcode latch to latch a test address ALU opcode included with the test command packet; and

- a test address ALU coupled to the test address latch and the test address ALU opcode latch for performing at least one of arithmetic and logic operations on the test address information in accordance with the test address opcode.

61. The memory test apparatus of claim 54 wherein the test circuit of the memory hub includes a test data generator comprising:

- a test data latch to latch test data information;

- a test data arithmetic and logic unit (ALU) opcode latch to latch a test data ALU opcode included with the test command packet; and

a test data ALU coupled to the test data latch and the test data ALU opcode latch for performing at least one of arithmetic and logic operations on the test data information in accordance with the test data opcode.

62. The memory test apparatus of claim 54 wherein the memory device interface of the memory hub comprises a memory device command latch, a memory device address latch and a memory device data latch for latching the memory device command, address, and data signals.

63. The memory test apparatus of claim 54 wherein the test clock frequency is less than the memory device clock frequency.

64. A memory test apparatus, comprising:  
a memory tester for providing memory test command packets to test memory devices;

a memory test bus coupled to the memory tester;

a memory module coupled to the memory test bus for testing, the memory module comprising:

a plurality of memory devices;

a memory device bus coupled to the memory devices; and

a memory hub coupled to the memory device bus, the memory hub

comprising:

a plurality of memory devices;

a memory device bus coupled to the memory devices; and

a memory hub coupled to the memory device bus, the memory hub

comprising:

a memory test bridge circuit having a tester interface through which test command packets are received responsive to a test clock signal and further having a

memory interface coupled to the tester interface through which memory commands corresponding to a test command packet are provided to at least one memory device responsive to a memory clock signal; and

an error detect circuit coupled to the memory test bridge circuit for comparing expected data received by the memory test bridge circuit to read data returned from the memory device in response to a memory command, the error detect circuit operable to generate in response to the comparison pass/fail data indicative of whether the read data matches the expected data.

65. The memory test apparatus of claim 64 wherein the test command packet comprises test command, test address, and test data signals, the test address signals representative of a memory device address and the test data signals representative of memory device data.

66. The memory test apparatus of claim 64 wherein the test command packet comprises test command, test address ALU opcode signals representative of at least one of arithmetic and logic operations performed to generate memory device address signals, and test data ALU opcode signals representative of at least one of arithmetic and logic operations performed to generate memory device data signals.

67. The memory test apparatus of claim 64 wherein the memory hub further comprises a capture buffer coupled to the test circuit and the memory device interface, the capture buffer configured to capture data read from the memory device under test and provide the same through the test circuit when requested.

68. The memory test apparatus of claim 64 wherein the test circuit of the memory hub is coupled to a plurality of uplinks on which a plurality of test command packets are received by the test circuit concurrently.

69. The memory test apparatus of claim 68 wherein the test circuit of the memory hub includes a multiplexer coupled to the plurality of uplinks to multiplex between the plurality of uplinks in providing the memory device command, address, and data signals to the memory device.

70. The memory test apparatus of claim 64 wherein the test circuit of the memory hub includes a test address generator comprising:

- a test address latch to latch test address information;
- a test address arithmetic and logic unit (ALU) opcode latch to latch a test address ALU opcode included with the test command packet; and
- a test address ALU coupled to the test address latch and the test address ALU opcode latch for performing at least one of arithmetic and logic operations on the test address information in accordance with the test address opcode.

71. The memory test apparatus of claim 64 wherein the test circuit of the memory hub includes a test data generator comprising:

- a test data latch to latch test data information;
- a test data arithmetic and logic unit (ALU) opcode latch to latch a test data ALU opcode included with the test command packet; and
- a test data ALU coupled to the test data latch and the test data ALU opcode latch for performing at least one of arithmetic and logic operations on the test data information in accordance with the test data opcode.

72. The memory test apparatus of claim 64 wherein the memory device interface of the memory hub comprises a memory device command latch, a memory device address latch and a memory device data latch for latching the memory device command, address, and data signals.

73. The memory test apparatus of claim 64 wherein the test clock frequency is less than the memory device clock frequency.

74. A method for testing a memory device, comprising:  
coupling test command packets from a tester to a memory hub responsive to a test clock signal having a test clock frequency;  
generating in the memory hub memory device command, address, and data signals in accordance with the test command packets; and  
coupling the memory device command, address, and data signals from the memory hub to a memory device under test responsive to a memory device clock signal having a memory device clock frequency.

75. The method of claim 74 wherein coupling test command packets from the tester to the memory hub comprises coupling test command, test address, and test data signals to the memory hub, the test address signals representative of a memory device address and the test data signals representative of memory device data.

76. The method of claim 74 wherein coupling test command packets from the tester to the memory hub comprises coupling test command signals, test address ALU opcode signals representative of at least one of arithmetic and logic operations performed to generate memory device address signals, and test data ALU opcode signals representative of at least one of arithmetic and logic operations performed to generate memory device data signals.

77. The method of claim 74, further comprising comparing read data from the memory device with expected data and generating a pass/fail signal indicative of the result of the comparison.

78. The method of claim 77, further comprising latching the read data from the memory device and providing the same for evaluation of the read data.

79. The method of claim 74 coupling test command packets from the tester to the memory hub comprises coupling a plurality of test command packets to the memory hub in parallel.

80. The method of claim 79 wherein generating memory device command, address, and data signals in accordance with the test command packets comprises selecting from the plurality of test command packets and generating memory device command, address, and data signals in accordance with the selected test command packet at a rate faster than the rate at which new test command packets are coupled to the memory hub in parallel.

81. The method of claim 74 wherein generating memory device address signals comprises performing at least one of arithmetic and logic operations in accordance with test address ALU opcodes included in the test command packets and wherein generating memory device data signals comprises performing at least one of arithmetic and logic operations in accordance with test data ALU opcodes included in the test command packets.

82. The method of claim 74 wherein the test clock frequency is less than the memory device clock frequency.

83. A method for testing a memory device, comprising:  
providing test command packets to a memory hub in parallel for testing a memory device under test; and

for each command packet provided to the memory hub in parallel, generating in the memory hub memory device command, address, and data signals in accordance with the selected test command packet and providing the memory device command, address, and data

signals to the memory device under test at a rate faster than which the test command packets are provided to the memory hub in parallel.

84. The method of claim 83 wherein providing test command packets from the tester to the memory hub comprises coupling test command, test address, and test data signals to the memory hub, the test address signals representative of a memory device address and the test data signals representative of memory device data.

85. The method of claim 83 wherein providing test command packets from the tester to the memory hub comprises coupling test command signals, test address ALU opcode signals representative of at least one of arithmetic and logic operations performed to generate memory device address signals, and test data ALU opcode signals representative of at least one of arithmetic and logic operations performed to generate memory device data signals.

86. The method of claim 83, further comprising comparing read data from the memory device with expected data and generating a pass/fail signal indicative of the result of the comparison.

87. The method of claim 86, further comprising latching the read data from the memory device and providing the same for evaluation of the read data.

88. The method of claim 83 wherein generating memory device address signals comprises performing at least one of arithmetic and logic operations in accordance with test address ALU opcodes included in the test command packets and wherein generating memory device data signals comprises performing at least one of arithmetic and logic operations in accordance with test data ALU opcodes included in the test command packets.

MEMORY HUB TESTER INTERFACE AND METHOD FOR USE THEREOF

## ABSTRACT OF THE DISCLOSURE

A memory hub including a memory test bridge circuit for testing memory devices. Test command packets are coupled from a tester to the memory hub responsive to a test clock signal having a test clock frequency. The test bridge circuit generates memory device command, address, and data signals in accordance with the test command packets, and the memory device command, address, and data signals are provided to a memory device under test that is coupled to the memory hub responsive to a memory device clock signal having a memory device clock frequency.

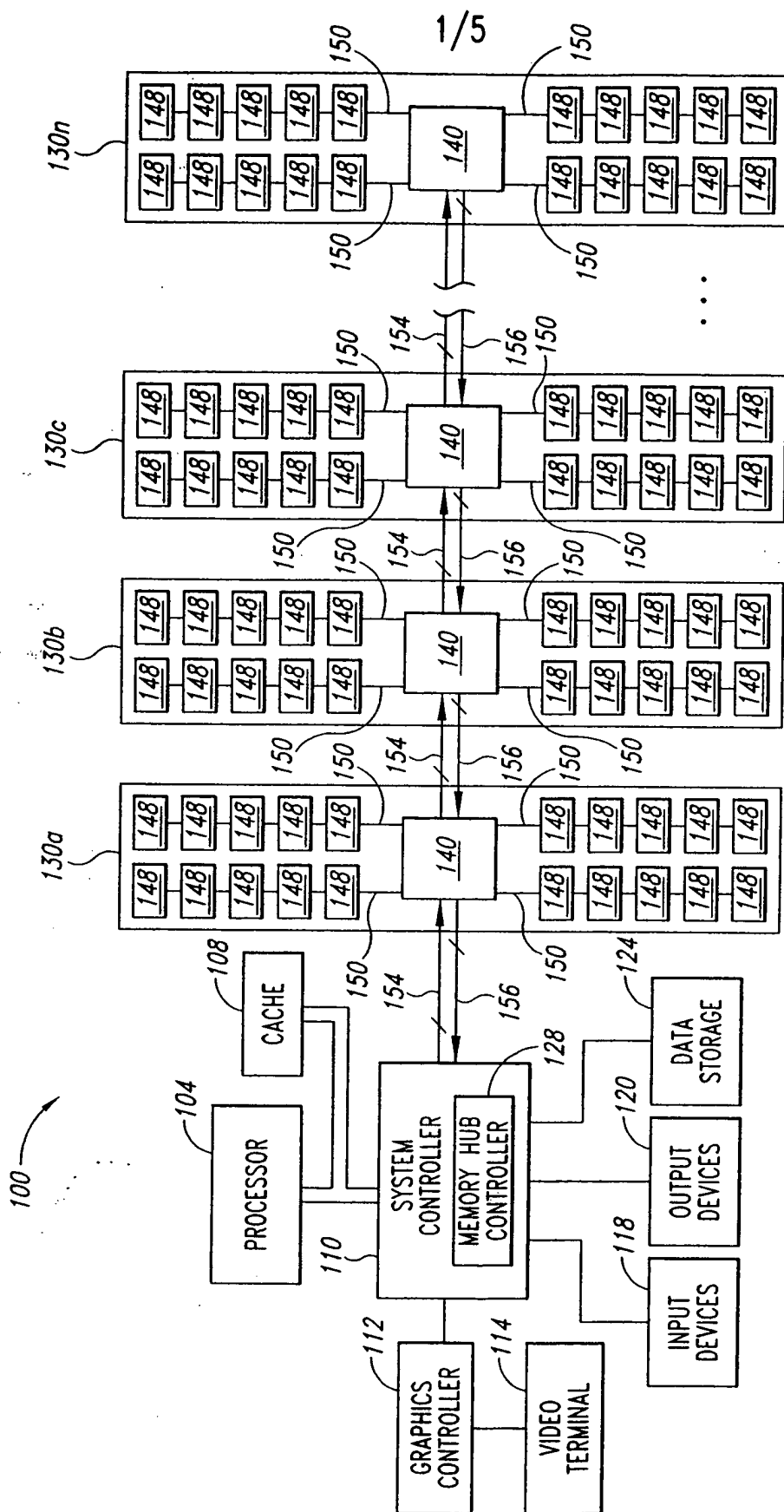
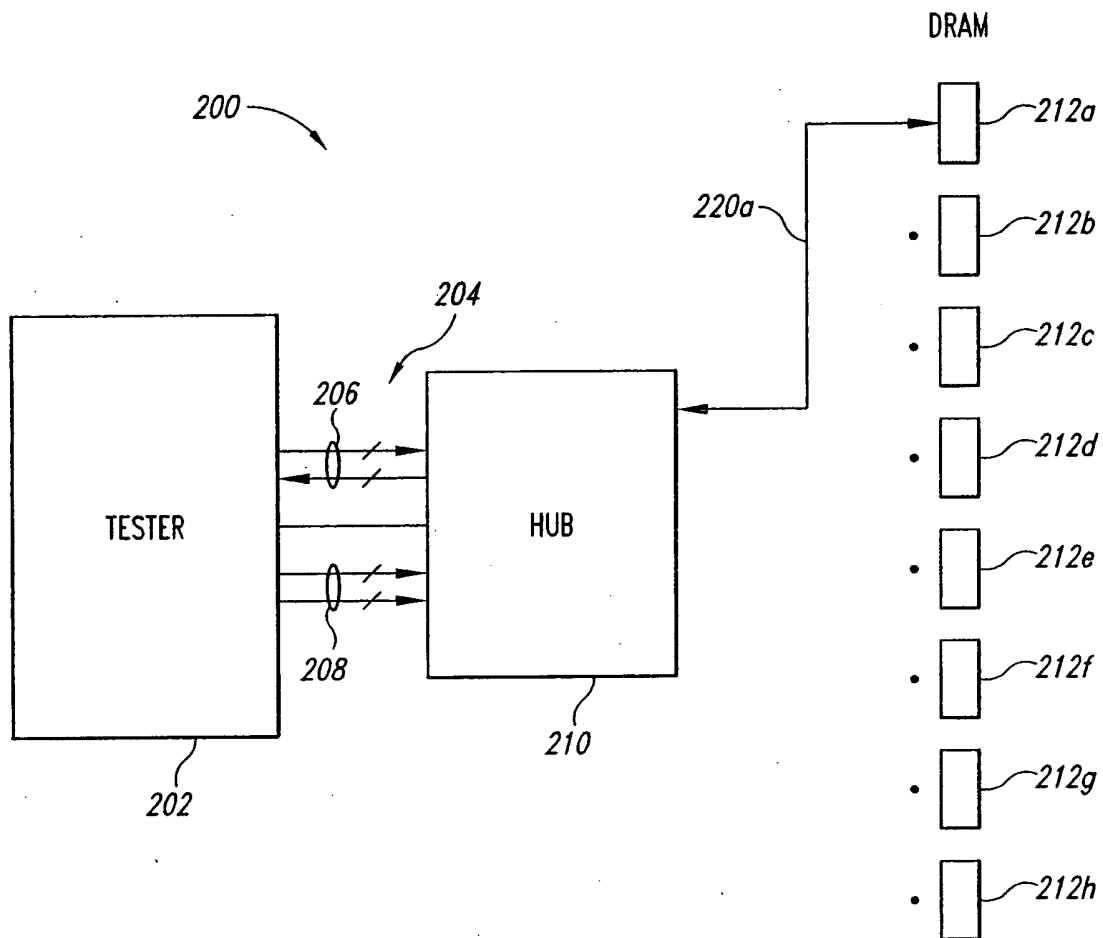


Fig. 1



*Fig. 2*

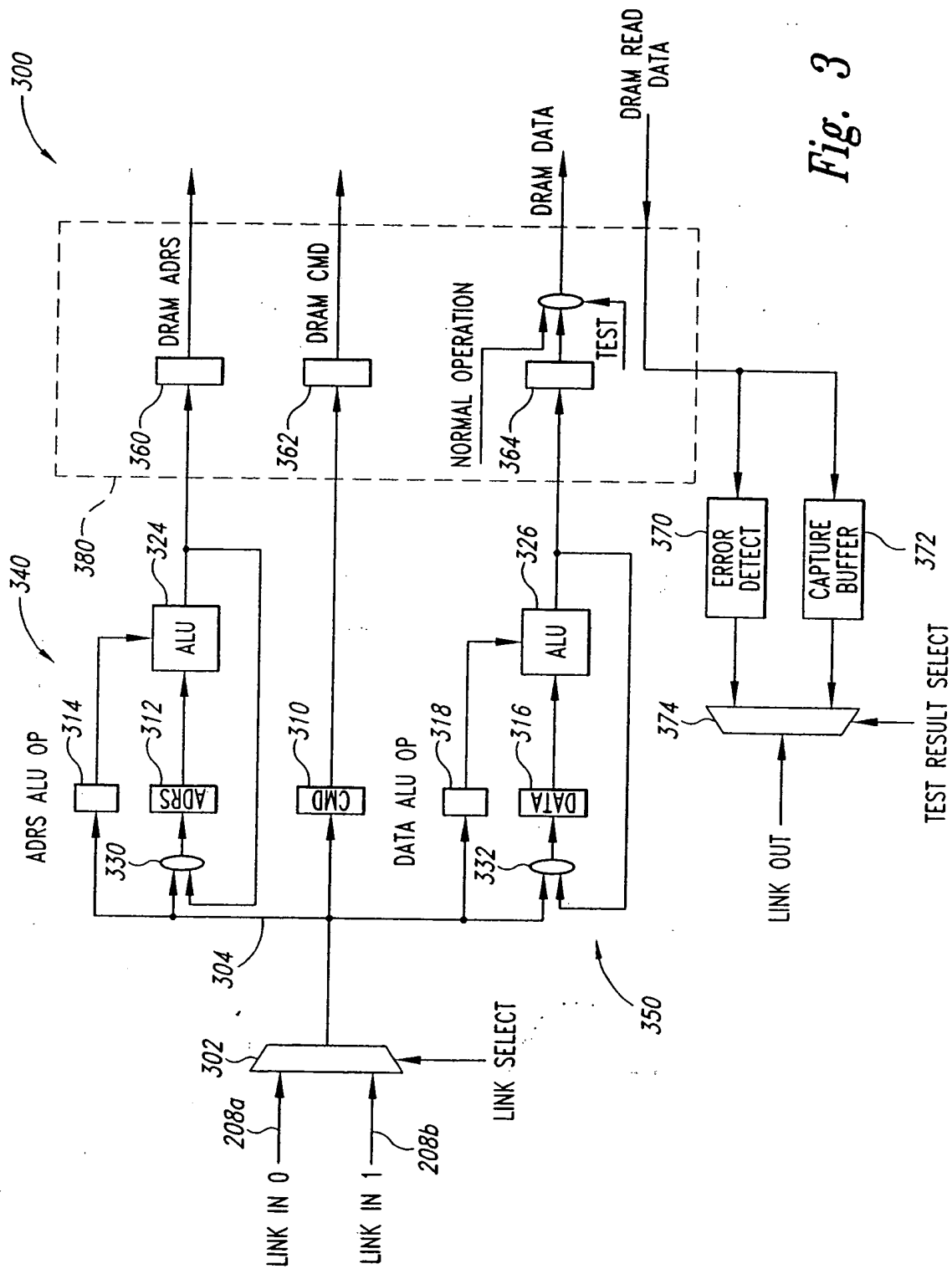


Fig. 3

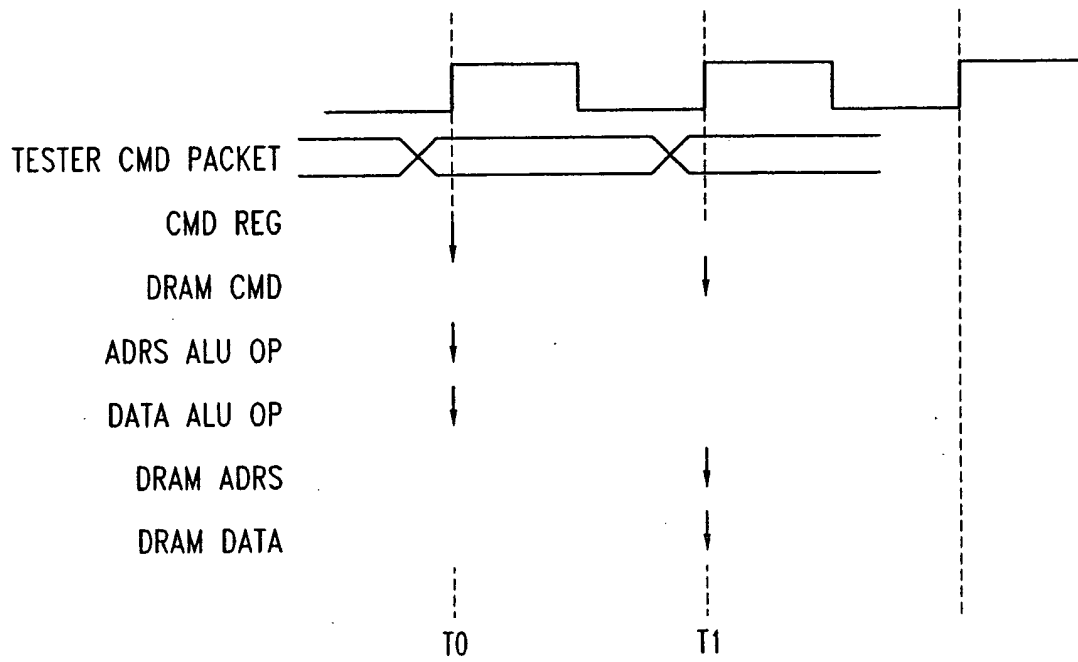


Fig. 4

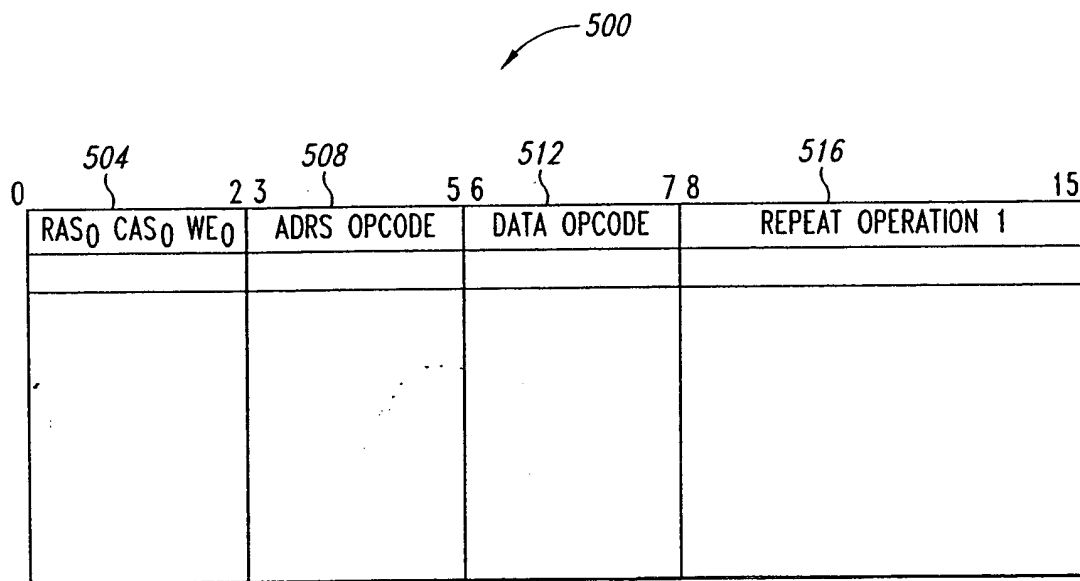


Fig. 5

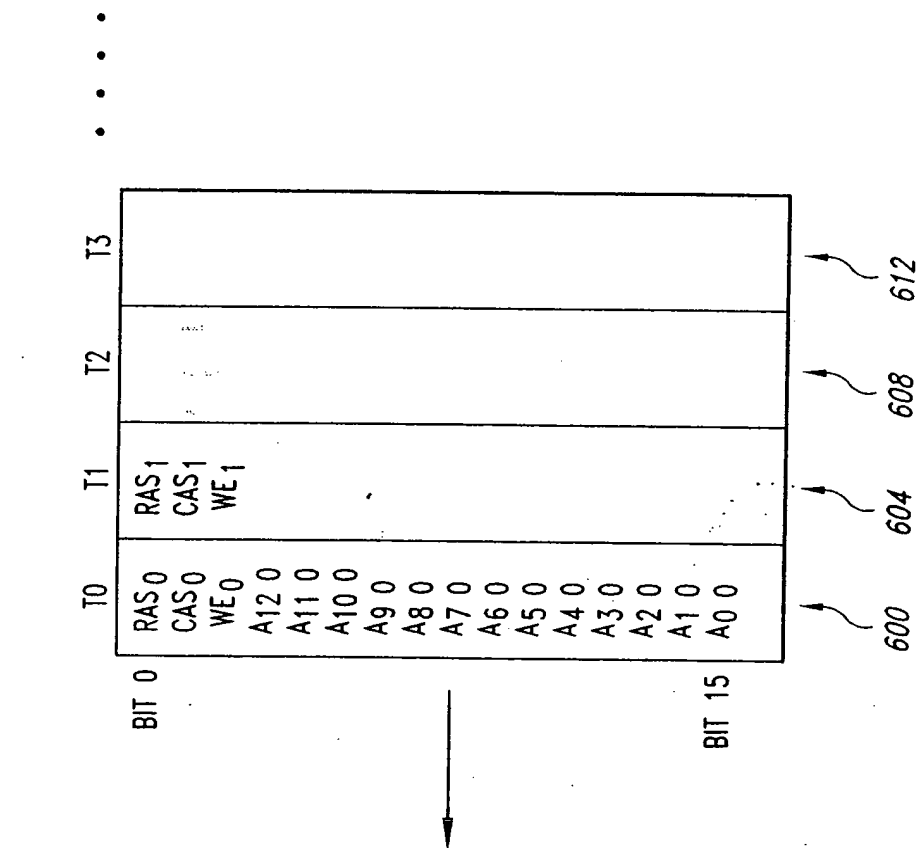


Fig. 6

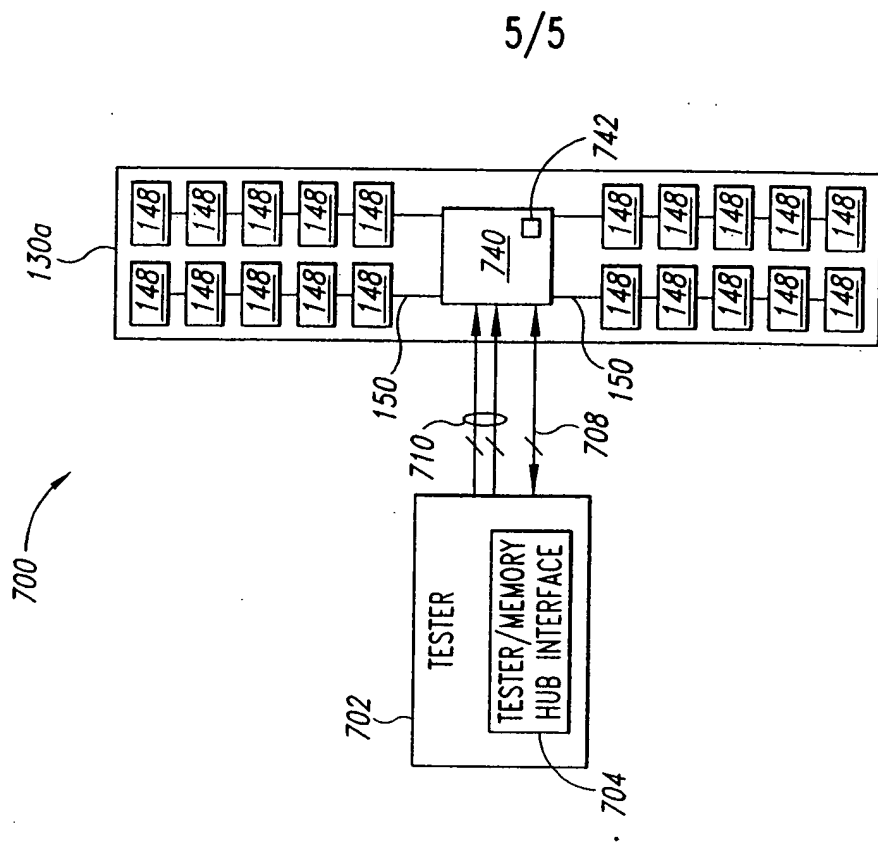


Fig. 7

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